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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/708,203 | 02/16/2004 | SHIH-CHANG SHEI | 11114-US-PA | 2202 |

31561 7590 10/05/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

| EXAMINER | |
|---|---|
| QUINTO, KEVIN V | |
| ART UNIT | PAPER NUMBER |
| 2826 | |

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/708,203 | SHEI ET AL. | |
| | Examiner | Art Unit | |
| | Kevin Quinto | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-18 and 21-26* is/are allowed.

6)☒ Claim(s) *1,3-8 and 19* is/are rejected.

7)☒ Claim(s) *2 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-8, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slater, Jr. et al. (USPN 6,791,119 B2) in view of Nitta et al. (United States Patent Application Publication No. US 2002/0163302 A1) and further in view of Oku et al. (USPN 6,497,944 B1).

3. In reference to claim 1, Slater, Jr. et al. (USPN 6,791,119 B2, hereinafter referred to as the "Slater" reference) discloses a similar device. Figure 4 of Slater illustrates a light emitting diode (LED) with a device substrate (110) and a first doped layer (120) formed on it. There is a light emitting layer (130) formed on the first doped layer (120). There is a second doped layer (140) formed on the light emitting layer (130). The first doped layer (120) is n-type while the second doped layer (140) is p-type; the two layers are both formed of a III-V semiconductor material. There is a transparent conductive oxide layer (412) on the second doped layer (150). There is a reflecting layer (414) on the transparent conductive oxide layer (412). There is an electrode (155) formed on the reflecting layer (414) and another electrode (160) formed on the first doped

layer (120). Slater does not disclose the use of a superlattice contact layer, however the use of such a layer is well known in the art. Nitta et al. (United States Patent Application Publication No. US 2002/0163302 A1, hereinafter referred to as the "Nitta" reference) discloses the use of a superlattice contact layer (126, figure 2) in order to decrease contact resistance (p.5, paragraph 75). Oku et al. (USPN 6,497,944 B1, hereinafter referred to as the "Oku" reference) discloses that lowering the contact resistance leads to a reduction in operating voltage which is a desired quality in light emitting devices (column 2, lines 19-25). In view of Nitta and Oku, it would therefore be obvious to use a superlattice contact layer in the device of Slater.

4. With regard to claim 3, Nitta discloses the use of a III-V p-type semiconductor multi-layer structure (p.5, paragraph 75).

5. In reference to claim 4, Slater discloses the use of gallium nitride as the semiconductor material (column 7, lines 36-41).

6. With regard to claim 5, Slater discloses the use of a quantum-well light emitting layer (column 7, lines 53-57).

7. In reference to claim 6, Slater meets the limitation of the claim (column 11, lines 30-34).

8. With regard to claim 7, the first doped layer (120) is n-type while the second doped layer (140) is p-type.

9. In reference to claim 8, Slater meets the limitation of the claim (column 7, lines 1-3).

10. In reference to claim 19, Slater (USPN 6,791,119 B2) discloses a similar device. Figure 4 of Slater illustrates a flip-chip light emitting diode (LED) with a package substrate (210). The LED device is face down and flipped on the package substrate. The LED device has a device substrate (110) and a first doped layer (120) formed on it. There is a light emitting layer (130) formed on the first doped layer (120). There is a second doped layer (140) formed on the light emitting layer (130). The first doped layer (120) is n-type while the second doped layer (140) is p-type; the two layers are both formed of a III-V semiconductor material. There is a transparent conductive oxide layer (412) on the second doped layer (140). There is a reflecting layer (414) on the transparent conductive oxide layer (412). There is an electrode (155) formed on the reflecting layer (414) and another electrode (160) formed on the first doped layer (120). Slater does not disclose the use of a superlattice contact layer, however the use of such a layer is well known in the art. Nitta (United States Patent Application Publication No. US 2002/0163302 A1) discloses the use of a superlattice contact layer (126, figure 2) in order to decrease contact resistance (p.5, paragraph 75). Oku (USPN 6,497,944 B1) discloses that lowering the contact resistance leads to a reduction in operating voltage which is a desired quality in light emitting devices (column 2, lines 19-25). In view of Nitta and Oku, it would therefore be obvious to use a superlattice contact layer in the device of Slater.

11. Claims 1, 3-7, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (United States Patent Application Publication

No. US 2004/0113156 A1) in view of Nitta et al. (United States Patent Application Publication No. US 2002/0163302 A1) and further in view of Oku et al. (USPN 6,497,944 B1).

12. In reference to claim 1, Tamura et al. (United States Patent Application Publication No. US 2004/0113156 A1, hereinafter referred to as the "Tamura" reference) discloses a similar device. Figure 4 of Tamura illustrates a light emitting diode (LED) with a device substrate (11) and a first doped layer (12) formed on it. There is a light emitting layer (13) formed on the first doped layer (12). There is a second doped layer (14) formed on the light emitting layer (13). The first doped layer (12) is n-type while the second doped layer (14) is p-type; the two layers are both formed of a III-V semiconductor material (p.4, paragraph 56). Tamura discloses (p.4, paragraphs 58-59) that there is a transparent conductive oxide layer (15) on the second doped layer (14). There is a reflecting layer (21) on the transparent conductive oxide layer (15). There is an electrode (22) formed on the reflecting layer (414) and another electrode (17) formed on the first doped layer (12). Tamura does not disclose the use of a superlattice contact layer, however the use of such a layer is well known in the art. Nitta (United States Patent Application Publication No. US 2002/0163302 A1) discloses the use of a superlattice contact layer (126, figure 2) in order to decrease contact resistance (p.5, paragraph 75). Oku (USPN 6,497,944 B1) discloses that lowering the contact resistance leads to a reduction in operating voltage which is a desired quality in light emitting devices (column 2, lines 19-25).

In view of Nitta and Oku, it would therefore be obvious to use a superlattice contact layer in the device of Tamura.

13. With regard to claim 3, Nitta discloses the use of a III-V p-type semiconductor multi-layer structure (p.5, paragraph 75).

14. In reference to claim 4, Tamura discloses the use of gallium nitride as the semiconductor material (p.4, paragraph 56).

15. With regard to claim 5, Tamura discloses the use of a quantum-well light emitting layer (p.4, paragraph 56).

16. In reference to claim 6, Tamura meets the limitation of the claim (p.4, paragraphs 58-59).

17. With regard to claim 7, the first doped layer (12) is n-type while the second doped layer (14) is p-type (p.4, paragraph 56).

18. In reference to claim 19, Tamura (USPN 6,791,119) discloses a similar device. Figure 4 of Tamura illustrates a flip-chip light emitting diode (LED) with a package substrate (20). The LED device is face down and flipped on the package substrate. The LED device has a device substrate (11) and a first doped layer (12) formed on it. There is a light emitting layer (13) formed on the first doped layer (12). There is a second doped layer (14) formed on the light emitting layer (13). The first doped layer (12) is n-type while the second doped layer (14) is p-type; the two layers are both formed of a III-V semiconductor material (p.4, paragraph 56). Tamura discloses (p.4, paragraphs 58-59) that there is a transparent conductive oxide layer (15) on the second doped layer (14). There is a reflecting layer (21) on the transparent conductive oxide layer

(15). There is an electrode (22) formed on the reflecting layer (21) and another electrode (17) formed on the first doped layer (12). Tamura does not disclose the use of a superlattice contact layer, however the use of such a layer is well known in the art. Nitta (United States Patent Application Publication No. US 2002/0163302 A1) discloses the use of a superlattice contact layer (126, figure 2) in order to decrease contact resistance (p.5, paragraph 75). Oku (USPN 6,497,944 B1) discloses that lowering the contact resistance leads to a reduction in operating voltage which is a desired quality in light emitting devices (column 2, lines 19-25). In view of Nitta and Oku, it would therefore be obvious to use a superlattice contact layer in the device of Tamura.

***Allowable Subject Matter***

19. Claims 9-18 and 21-26 are allowed.

20. Claims 2 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

21. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a flip-chip light emitting diode (LED) package with a package substrate and an LED (which is face down and inverted on the package substrate) that has the following layer structure: device substrate, a first doped layer made of a III-V semiconductor material of a first conductivity type (having an electrode), a light emitting layer, a second doped layer made of a III-V

semiconductor material of a second conductivity type, a strained superlattice contact layer, a transparent conductive oxide layer, a transparent insulating layer, and a reflecting layer (having an electrode).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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